REMARKS

Amendments

Claims 1, 9, and 12 were amended to incorporate the write latch from dependent claims 2, 10, and 16, respectively. Claims 1, 7, 9, and 12 were also amended to include a single set of sense amplifiers in a read/write circuit. Claim 17 was amended to correct a typographical error. Claims 2, 10, and 16 were cancelled without prejudice.

Rejections Under 35 U.S.C. § 103

The Advisory Action maintains the rejections of the Final Office Action.

Specifically, the Advisory Action and Final Office Action rejected claims 1-10, and 12-20 under 35 U.S.C. § 103 as being unpatentable in view of Hazen et al. (U.S. Patent 6,088,264). Claims 2, 10, and 16 were cancelled hereby without prejudice or disclaimer. Applicant respectfully traverses this rejection and feels that claims 1, 3-9, 12-15, and 17-20, as amended, are allowable for the following reasons.

Applicant respectfully maintains that Hazen et al. teaches a memory which has a separate read/write circuit for each partition. As such, the Applicant submits that Hazen et al. does not disclose or suggest a memory with a read/write circuit having a single set of read/write sense amplifiers, wherein the read/write circuit supports multiple simultaneous read/write operations. Hazen et al. teaches away from having a single set of sense amplifiers, each read/write circuit of Hazen et al. has its own set of sense amplifiers and is restricted to executing a single operation at any given time period. *See, e.g.*, Hazen et al., Figure 2, and column 2, line 47 to column 3, line 24. Applicant therefore respectfully submits that Hazen et al. does not teach or suggest a non-volatile memory device with a non-volatile memory array, read/write circuitry having a set of sense amplifiers coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks, and a write latch coupled to the read/write circuitry, wherein the write latch is adapted to store the first data provided on external data communication connections, as maintained by the Examiner.

In addition to the above argument regarding Hazen et al. disclosing a memory device having a memory device with a plurality of read/write circuits, the Applicant further contends that there is no motivation or suggestion to modify the reference in this manner. Specifically, Applicant contends that to modify Hazen et al. to provide writing to a first bank of a memory array while reading from two or more remaining banks of the memory array would require a modification of Hazen et al.'s user interface and plurality of read/write circuitry to allow the writing to a first bank of a memory array while reading from two or more remaining banks of the memory array with a single read/write circuit having a single set of sense amplifiers. Hazen et al. expressly teaches away from parallel read and write operations using the same set of sense amplifiers, each read/write circuit of Hazen et al. has its own set of sense amplifiers and is restricted to executing a single operation at any given time period. *See, e.g.*, Hazen et al., column 2, line 65 to column 3, line 24. Applicant also finds no motivation or suggestion to modify the operation of Hazen et al. expressly or impliedly contained in the Hazen et al. reference, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Applicant thus submits that the Office has also failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

Applicant's claim 1 recites, in part, "read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks" and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits

that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 1.

Applicant's claim 7 recites, in part, "read/write circuitry coupled to the array, wherein the read/write circuitry writes the first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks" and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 7.

Applicant's claim 9 recites, in part, "read/write circuitry coupled to the array, wherein the read/write circuitry writes first data provided by the processor to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks and provides the second data to the processor" and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 9.

Applicant's claim 12 recites, in part, "writing first data to a first bank location," "substantially simultaneously reading second data from a second bank location," "substantially simultaneously reading third data from a third bank location," and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Hazen et al. fails to teach or suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 12.

Applicant's claim 17 recites, in part, "writing the first data from the write latch to a first bank location," "substantially simultaneously reading second data from a second bank location," "substantially simultaneously reading third data from a third bank location," and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Hazen et al. fails to teach or

suggest such a memory device. As such, Hazen et al. fails to teach or suggest all elements of independent claim 17.

Applicant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 1, 7, 9, 12, and 17, as amended, and, in addition, that claims 1, 7, 9, 12, and 17 as pending have been shown to be patentably distinct from the cited reference, either alone or in combination with the Examiner's taking of official notice. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1, 7, 9, 12, and 17. As claims 3-6, 8, 13-15, and 18-20 depend from and further define claims 1, 7, 9, 12, and 17, respectively, they are also believed to be allowable.

The Advisory Action and Final Office Action rejected claims 1-10, and 12-20 under 35 U.S.C. § 103 as being unpatentable in view of Nawaki (U.S. Patent 6,081,450). Claims 2, 10, and 16 were cancelled hereby without prejudice or disclaimer. Applicant respectfully traverses this rejection and feels that claims 1, 3-9, 12-15, and 17-20, as amended, are allowable for the following reasons.

Applicant respectfully maintains that Nawaki teaches a non-volatile memory where the word lines of the array can be split through the use of pass gates between memory blocks, where differing memory blocks can be independently accessed through separate word line decoders at opposite ends of the split word lines of the array allowing simultaneous operations to be performed on opposite sides of the split word lines by separate read/write circuits, having separate row decoders and separate sets of sense amplifiers. As such, the Applicant submits that the memory disclosed in Nawaki can only simultaneously execute a single read and write operation at a time and that Nawaki teaches away from having a single set of sense amplifiers. The Applicant therefore respectfully submits that Nawaki does not teach or suggest a non-volatile memory device with a non-volatile memory array, read/write circuitry having a single set of sense amplifiers coupled to the array, wherein the read/write circuitry writes first data to a first

one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks, and a write latch coupled to the read/write circuitry, wherein the write latch is adapted to store the first data provided on external data communication connections, as maintained by the Examiner. *See, e.g.*, Nawaki, Figure 1, Figure 3, column 6, lines 3-13, and column 7, line 59 to column 8, line 4.

In addition to the above arguments regarding Nawaki not teaching or suggesting writing to a first bank of a memory array while reading from two or more remaining banks of the memory array, the Applicant further contends that there is no motivation or suggestion to modify the reference in this manner. Specifically, Applicant contends that to modify Nawaki to provide writing to a first bank of a memory array while reading from two or more remaining banks of the memory array would require a modification of Nawaki's read/write circuitry to reduce the sense amplifiers to a single set of sense amplifiers and to incorporate a write latch and to allow the latching of write data and writing to a first bank of a memory array while reading from two or more remaining banks of the memory array. Nawaki expressly teaches away from parallel read and write operations using the same set of sense amplifiers, each row decoder circuit of Nawaki has its own set of sense amplifiers and is restricted to executing a single operation at any given time period. *See, e.g.*, Nawaki, Figure 1, Figure 3, column 6, lines 3-13, and column 7, line 59 to column 8, line 4. Applicant also finds no motivation or suggestion to modify the operation of Nawaki expressly or impliedly contained in the Nawaki reference, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Applicant thus submits that the Office has also failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of

reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

Applicant's claim 1 recites, in part, "read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks" and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 1.

Applicant's claim 7 recites, in part, "read/write circuitry coupled to the array, wherein the read/write circuitry writes the first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks" and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 7.

Applicant's claim 9 recites, in part, "read/write circuitry coupled to the array, wherein the read/write circuitry writes first data provided by the processor to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks and provides the second data to the processor" and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 9.

Applicant's claim 12 recites, in part, "writing first data to a first bank location," "substantially simultaneously reading second data from a second bank location," "substantially simultaneously reading third data from a third bank location," and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Nawaki fails to teach or suggest

such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 12.

Applicant's claim 17 recites, in part, "writing the first data from the write latch to a first bank location," "substantially simultaneously reading second data from a second bank location," "substantially simultaneously reading third data from a third bank location," and "wherein the read and write operations utilize the same set of read/write sense amplifiers." As detailed above, Applicant submits that Nawaki fails to teach or suggest such a memory device. As such, Nawaki fails to teach or suggest all elements of independent claim 17.

Applicant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 1, 7, 9, 12, and 17, and, in addition, that claims 1, 7, 9, 12, and 17 as pending have been shown to be patentably distinct from the cited reference, either alone or in combination with the Examiner's taking of official notice. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1, 7, 9, 12, and 17. As claims 3-6, 8, 13-15, and 18-20 depend from and further define claims 1, 7, 9, 12, and 17, respectively, they are also believed to be allowable.

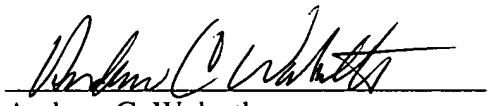
CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. No new matter has been added and no additional fee is required by this amendment and response.

The Examiner is invited to contact Applicant's representative at the number below if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

Date: 7/7/04



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